关于APU外接 LDDDR4X@3733bps的LB设计

与仿真分析

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关于LPDDR4X

	DDR4	LPDDR4	LPDD4X
VDDQ	1.2V	1.1V	0.6V
Data rate(Gbps)	3200	4266	4266

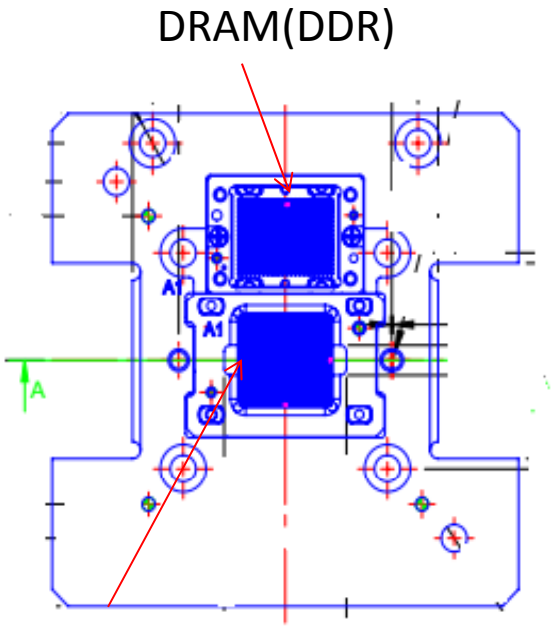
DDR4是面向桌面的应用，而LPDDR4则是面向移动的应用。LPDDR4可以到32Gb容量, 速率高达4266Gbps; LPDDR4X则将IO电压降到0.6V， 以进一步减少功耗。

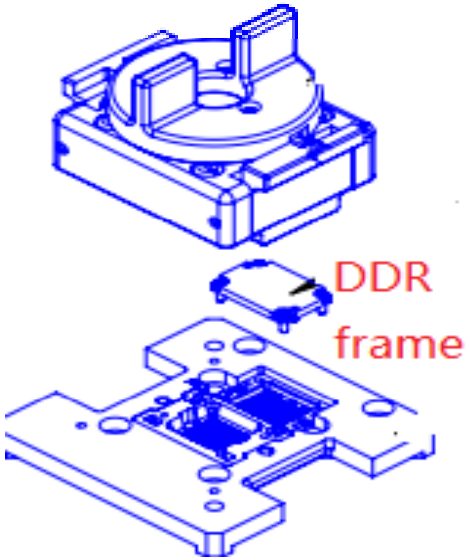
AP（应用处理器）为手机核心芯片，新一代智能手机要支持LPDDR4X。

LB测试方案

- APU外接LPDDR4X，速度满足3733Mbps;
- 考虑将APU与DDR模组放于同一socket上。
- 通过仿真分析研究信号是否能满足要求。

socket方案





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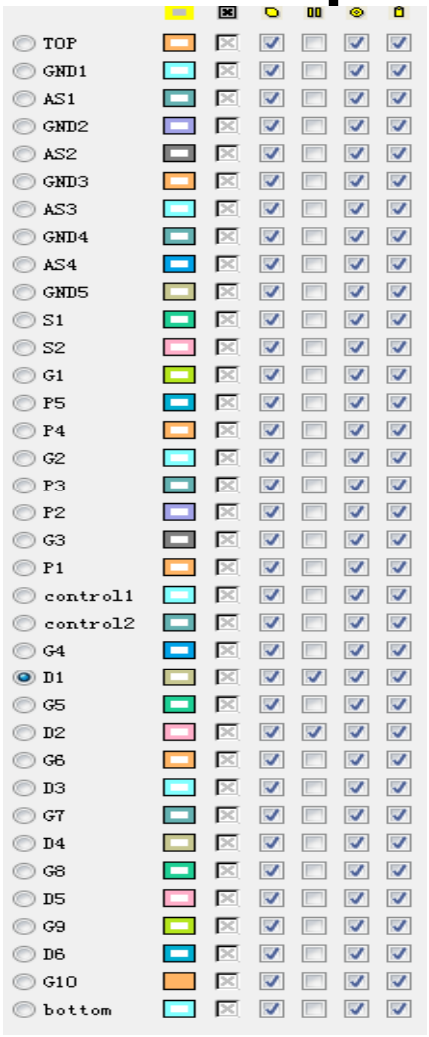
stackup



36 layers, board thickness 175Mils

Layout rule

BGA area breakout width: 2.5mil (58 Ohm);

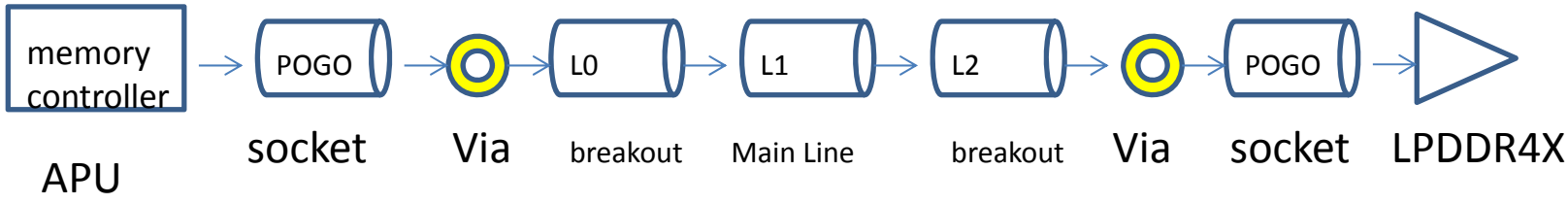
Main line width: 5Mil (42 Ohm);

Differential: 5/10/5Mil, 83 Ohm;

Trace space: 10Mil or 2X trace width;

仿真

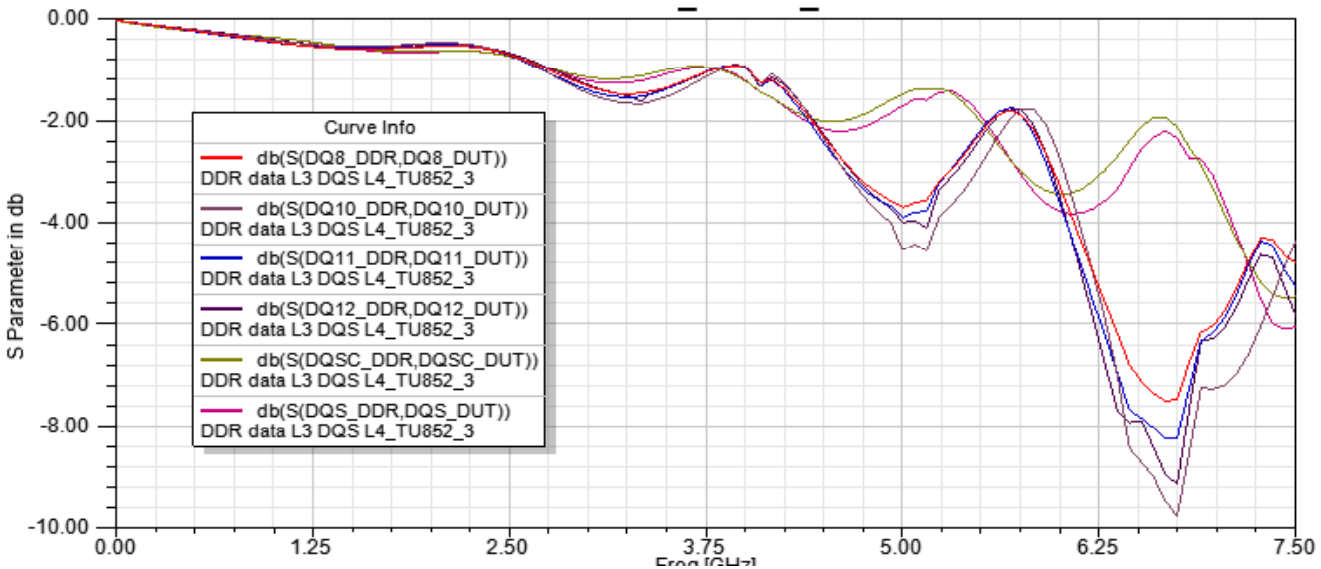
通路

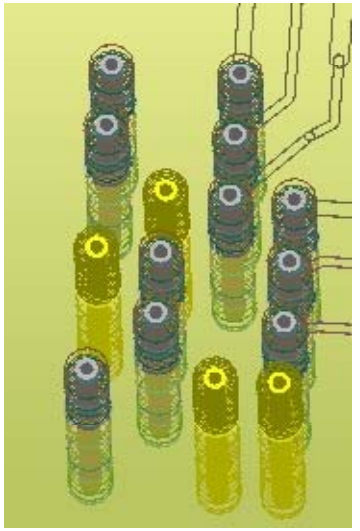


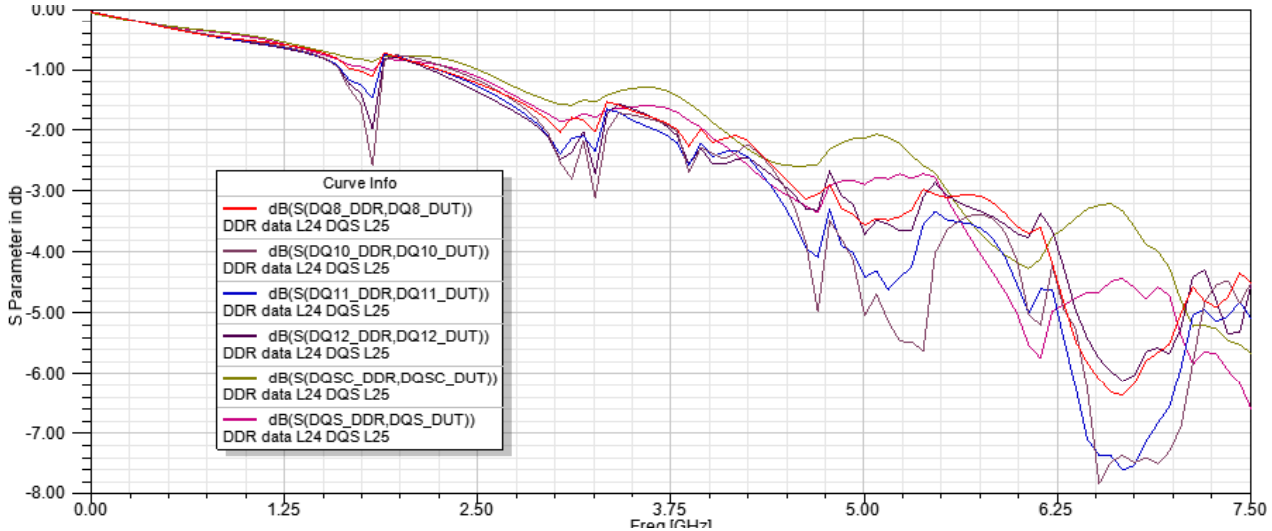
socket模型

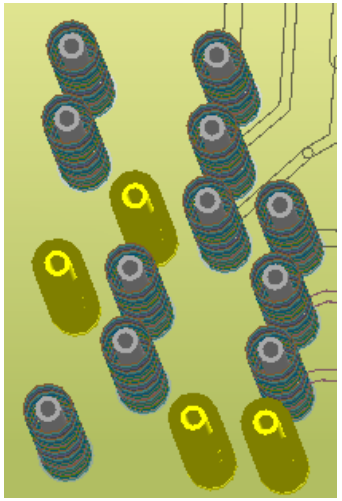
通常厂家提供的参数是基于GSG排列， 实际情况不可能这么理想， 按1.5nH电感和 0.5pF电容估算

insertion loss - trace in L3/L5 or L23/L25

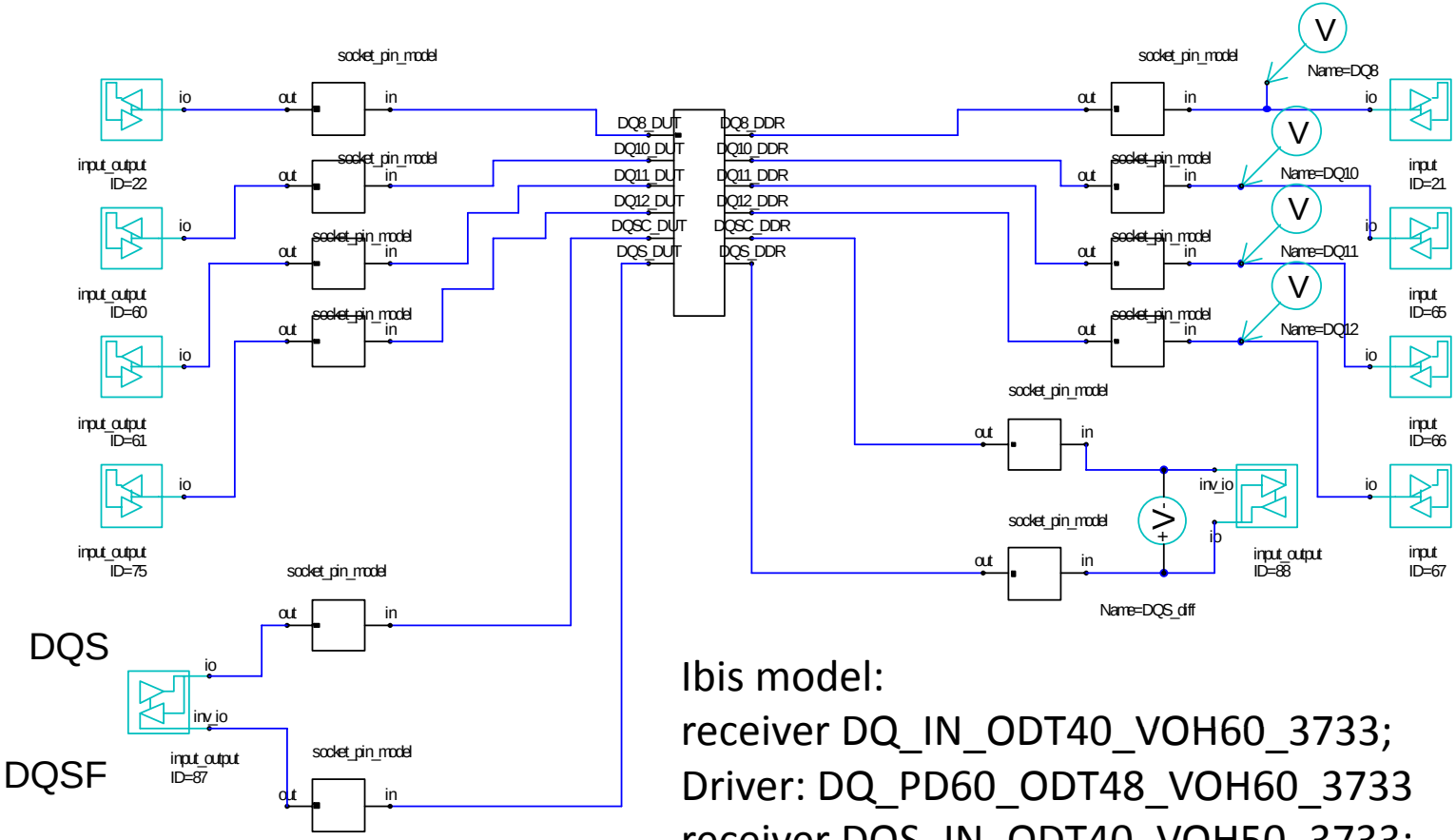








仿真电路



Ibis model:

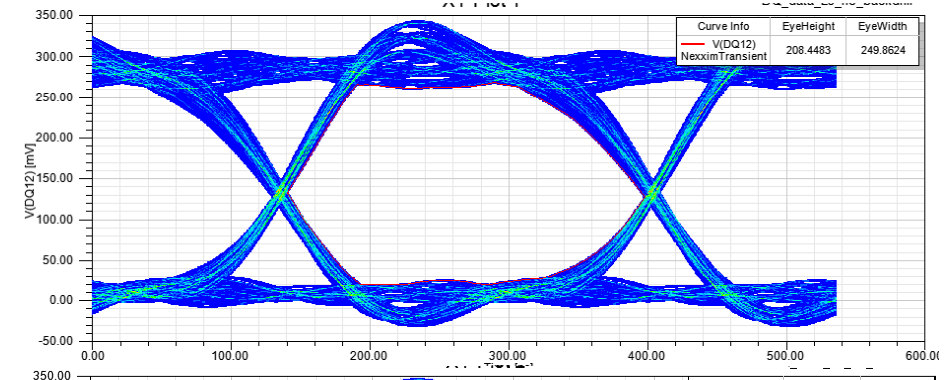
receiver DQ_IN_ODT40_VOH60_3733;

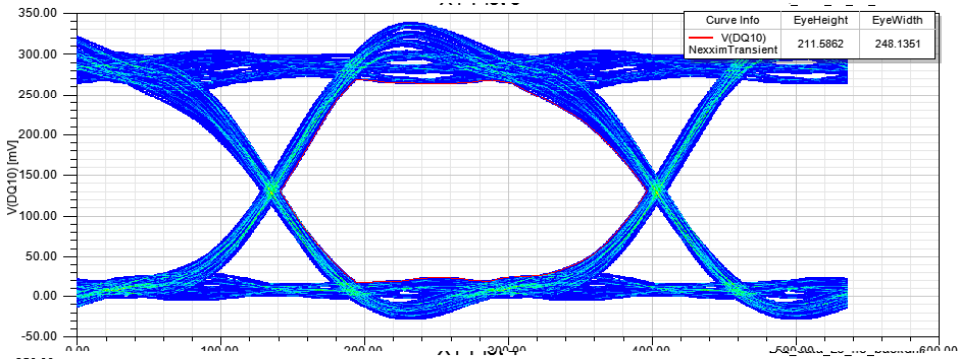
Driver: DQ_PD60_ODT48_VOH60_3733

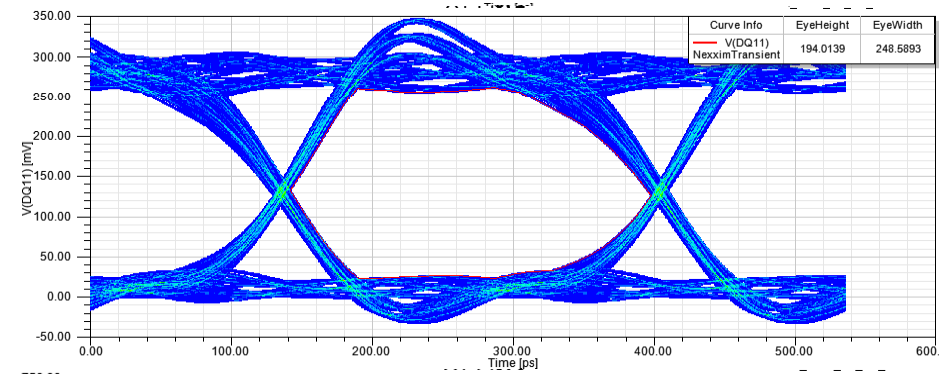
receiver DQS_IN_ODT40_VOH50_3733;

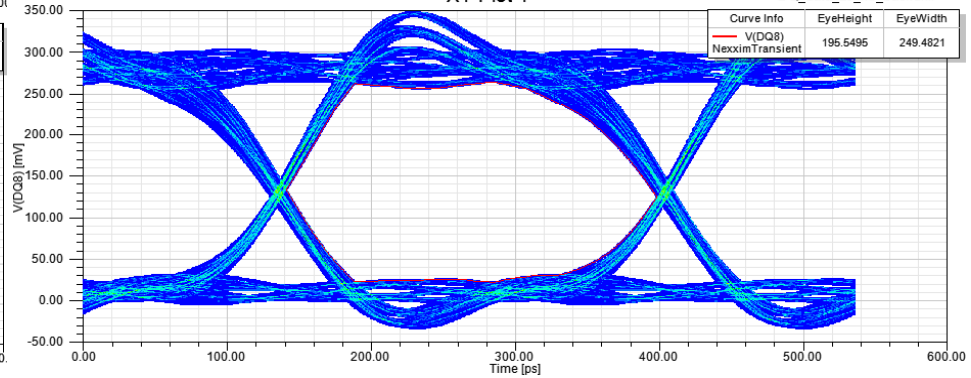
Driver: DQS_PD40_ODT40_VOH50_3733

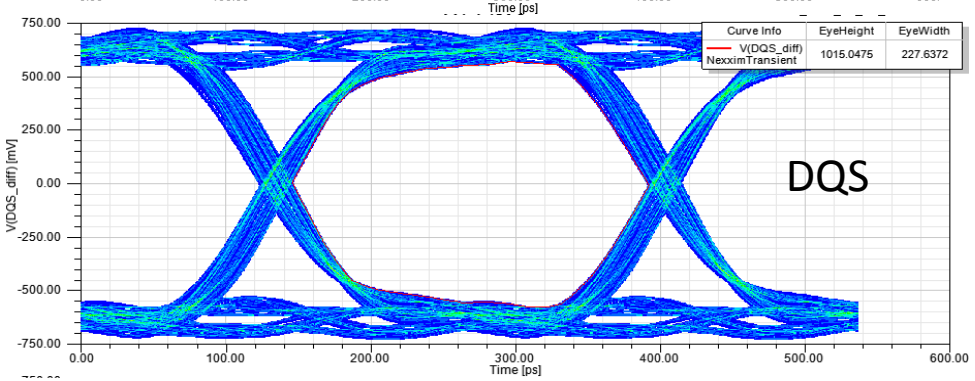
DQ Trace in L3/L5





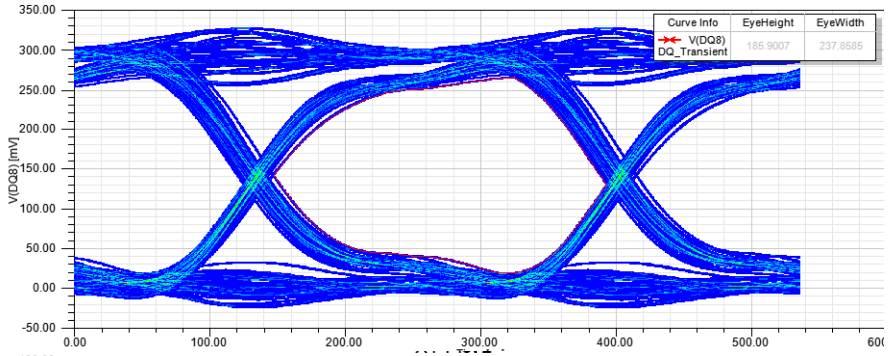


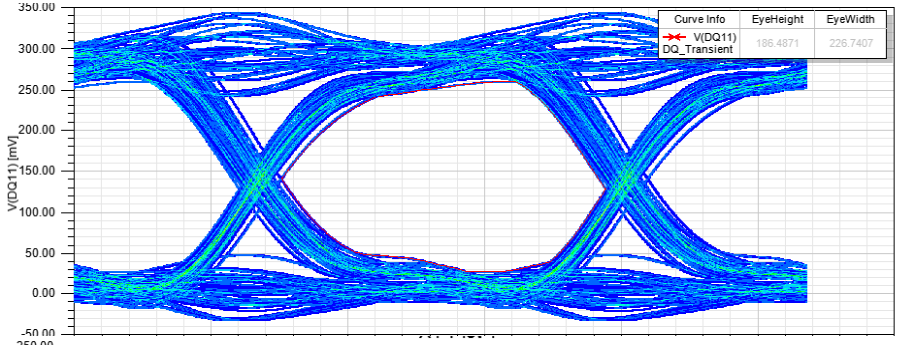


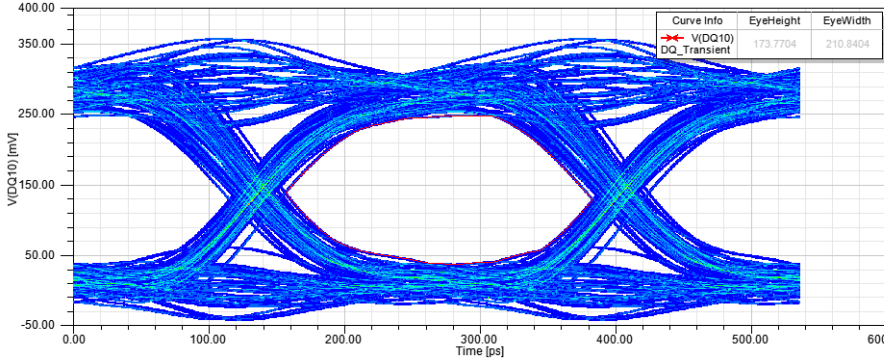


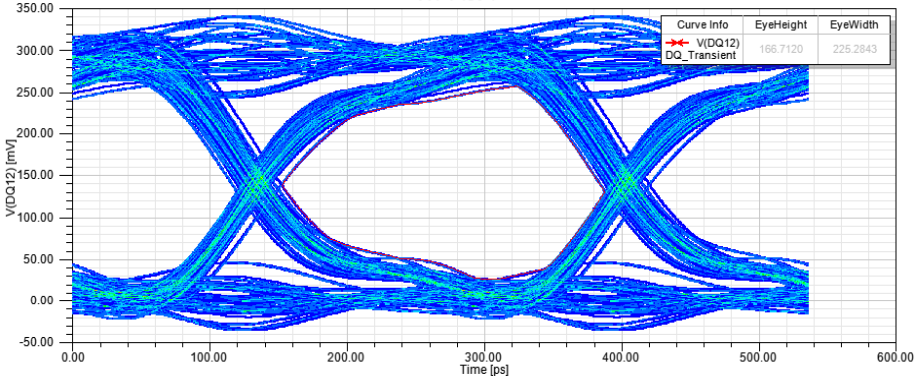
3733Gbps

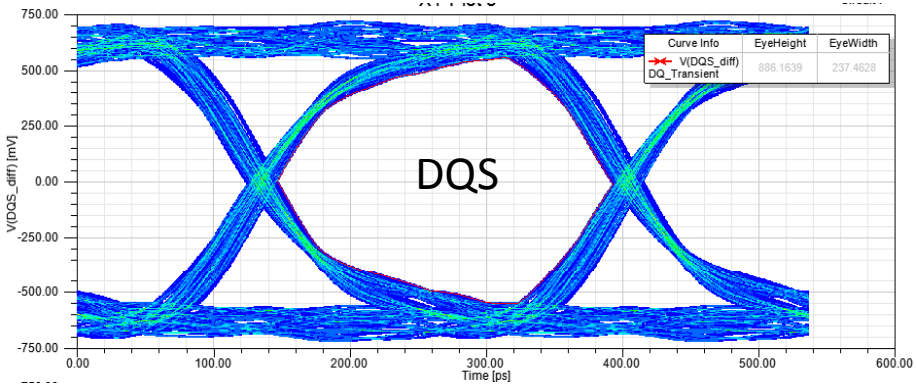
DQ Trace in L23/L25





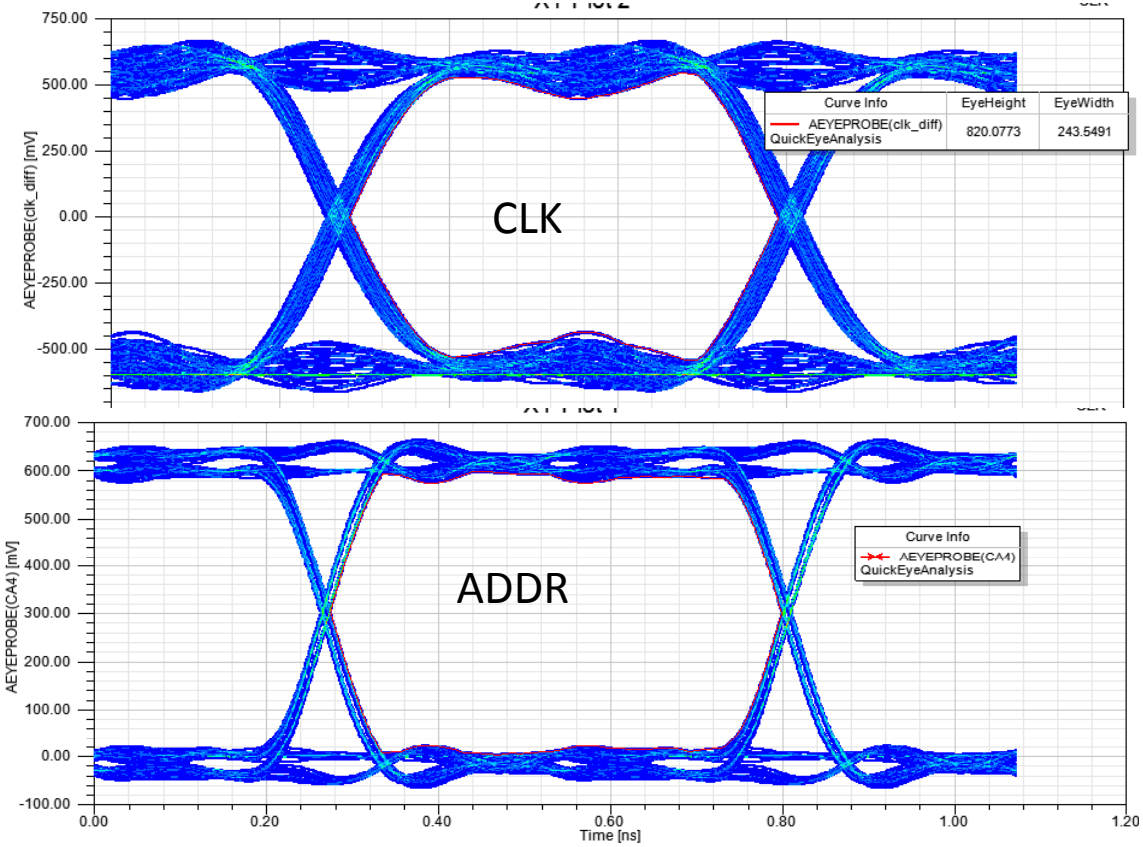


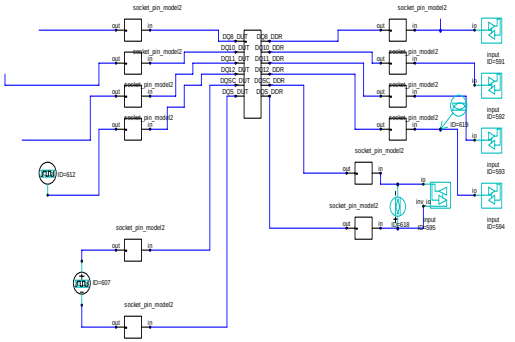




3733Gbps

CLK and address





CLK Input differential: 1.2Vp-p;1866MHz

Address input: 0.6Vp-p;1866bps;

Driving by PRBS pattern with 50 Ohm source impedance

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结论

- DDR走线在PCB上部时比在下部损耗小；
- DDR线在PCB上部时比在下部眼图眼裂更大；
- DDR走线在PCB上部时比在下部信号过冲大；如能去掉多余的stub则更佳。
- DUT和DRAM处的过孔和PCB板的厚度是信号变坏的原因。
- 采用2.5MIL(BGA 出线），单线5MIL/45+/-10%欧；差分90欧+/10%，线距10MIL，可以达成3733bps速率。